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EXAMINER

GARCIA OTERO, EDUARDO

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/410,160

Applicant(s)

BELL ET AL.

Examiner

Eduardo Garcia-Otero

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 September 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION-Final

Introduction

1. Title is: METHOD AND APPARATUS FOR AUTOMATED ENUMERATION, SIMULATION, IDENTIFICATION AND/OR IRRADIATION OF DEVICE ATTRIBUTES
2. First Named Inventor is: BELL
3. Claims 1-20 are pending, and have been examined and rejected.
4. This is the second action on the merits, and is a Final Action.

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5. **Sample** refers to Sample et al. US Patent 5,841,967 filed 10/17/96, issued 11/24/98.
6. **Tzori** refers to Tzori US Patent 6,202,044 B1 filed 6/12/98, issued 3/13/01.
7. **Higgins** refers to Higgins et al. US Patent 6,397,349 B2 filed 10/13/98, issued 5/28/02.
8. **Kablanian** refers to Kablanian et al. US Patent 5,764,878, filed 2/7/96, and issued June 9, 1998.

Drawings-draftperson objection-pending

9. **This application has been filed with informal drawings** which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. Specifically, Form 948, Notice of Draftperson's Drawing Patent Review was sent with the previous action.

REMARKS-Specification-objections-some withdrawn

10. Examiner's prior objections are withdrawn due to Applicant's amendments, with one exception.

11. It is not clear whether FIG 2 refers to the same embodiment as FIG 1. The amendments clarify that FIG 3 refers to the same embodiment as FIG 1, but do not clarify the relationship of FIG 2. Please clarify whether FIG 2 refers to the same embodiment as FIG 1. If FIG 2 does not refer to the same embodiment as FIG 1, then please clearly state the differences between the embodiment of FIG 1 and the embodiment of FIG 2.

REMARKS-Drawings-examiner's objections-withdrawn

12. Examiner's prior objections are withdrawn due to Applicant's amendments.

REMARKS-Claim Rejections - 35 USC § 112- first paragraph-description

13. Examiner's prior rejections are withdrawn due to Applicant's amendments and persuasive arguments.

REMARKS-Claim Rejections - 35 USC § 112-Second Paragraph-indefinite

14. Examiner's prior rejections are withdrawn due to Applicant's amendments and persuasive arguments.

REMARKS-Claim Rejections - 35 USC § 102(e)

15. **Remarks Page 22, last full paragraph.** Applicant unpersuasively asserts that Sample "appears to be silent regarding **enumerating** fuses in a design", and asserts that Sample transforms "a netlist of gates and flip-flops into transistor equivalents or library cells". Applicant mischaracterizes Sample. Sample states (quote) "transforms the netlist of gates and flip-flops into a transistor list or layout....the transistor list or layout specification is used to burn [sic] fuses of a programmable device" at Column 1 line 38. Note that Merriam-Webster's Collegiate Dictionary, Tenth Edition, defines "enumerate" as "to ascertain the number of: COUNT" or "to specify one after another: LIST". Thus, the

plain language meaning of enumerate is to count or to list. Note that at a minimum, Sample's transistor list or layout specification contains the number (count) of fuses of a programmable device that must be burned.

16. **Remarks Page 23, first full paragraph.** Applicant unpersuasively asserts that Sample does not disclose "**compiling** data for each of the fuses". Note that, at a minimum, Sample compiles data on each fuse regarding whether or not to burn the fuse.
17. **Remarks Page 23, last full paragraph.** Applicant asserts that Sample "appears to be silent about repairing a design by programming a fuse", and contrasts "**programmed for a repair to verify the repair**" from Sample's discussion of "manufactured". This regards an amendment added to Claim 1 (amended), so it will be addressed below in the new rejections.
18. **Remarks Page 24, first full paragraph.** Applicant unpersuasively asserts that Sample "does not appear to disclose or suggest **schematic instance paths**" as claimed in Claim 4. The Specification does not mention or define "schematic instance paths". Therefore, the Examiner will interpret these as simply as simply paths or routes. Further, a rejection for indefiniteness is made (below) for Claim 4.
19. **Remarks Page 25, first full paragraph.** Applicant unpersuasively asserts that sample does not disclose "generating a **fuse report**". Note that Merriam-Webster's Collegiate Dictionary, Tenth Edition, defines "report" as "to give an account of: RELATE" or "**to describe as being in a specified state**" or "to serve as a carrier of" or "to make a written record or summary of" and so forth. Sample uses the transistor list or layout specification

to burn fuses. Therefore, Sample's "transistor list or layout specification" describes the state of certain fuses as being burned.

20. **Remarks Page 25, second full paragraph.** Applicant persuasively asserts that burning fuses does not inherently require a "fuse report". Applicant asserts that fuses can be selected manually for burning. This inherency argument will not be used in the new rejection to amended Claim 5.

21. **Remarks Page 25, third full paragraph.** Applicant unpersuasively asserts "Physical locations of fuses in a programmable device programmed per a design are not the same as physical locations of a device in the design itself". This assertion/distinction is not clear, and its application to the rejection of Claim 6 is not clear.

REMARKS-Claim Rejections - 35 USC § 103

22. Most of the claims rejected as obvious have been substantially amended.

23. Remarks Page 27, first full paragraph. Claim 7 has been substantially amended, and will receive a new rejection.

Drawings-objections

24. FIG 3 contains logical errors. The element 316 branches in two different directions simultaneously when the condition is NO. Specifically, element 316 branches simultaneously to the left to element 318, and to the right to element 320. Also, elements 318 and 320 are conditional branches, but each has only one path leaving. A conditional branch must have at least 2 paths leaving. Please correct these logical errors.

Claim Rejections - 35 USC § 112-First Paragraph-enablement

25. The following is a quotation of the first paragraph of 35 U.S.C. 112: The specification shall contain a written description of the invention, and of the manner and process of making and using it, in

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such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

26. **Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph**, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
27. Claims 1-20 are rejected because FIG 3 contains logical errors, as discussed above.
28. Claim 1 states “**simulating said design with at least one of said fuses programmed for said repair to verify said repair**”. The specification does not adequately describe this phrase.
29. Claim 4 (amended) states “**schematic instance paths**”. The specification does not adequately describe this phrase.
30. Claim 7 (amended) states “**generating a repair file that predicts said at least one of said fuses programmed for said repair**”. The specification does not adequately describe this phrase.
31. Claim 10 (amended) states “**listing an output of said repair program as a list of coordinates for said at least one of said fuses programmed for said repair in terms of a plurality of logical addresses**”. The specification does not adequately describe this phrase.
32. Claim 18 states “**said first circuit is further configured to provide an elevation of said fuses at least one level of abstraction in said design**”. The specification does not adequately describe this phrase.

33. Claim 19 states **“said first circuit is further configured to collect data relevant to said fuses that are grouped”**. The specification does not adequately describe this phrase.

Claim Rejections - 35 USC § 112-Second Paragraph-indefinite

34. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
35. **Claims 1, 4, 7, 18, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
36. Claim 1 (amended) states **“simulating said design with at least one of said fuses programmed for said repair to verify said repair”**. This phrase is not adequately defined.
37. Claim 4 (amended) states **“schematic instance paths”**. This phrase is not adequately defined.
38. Claim 7 (amended) states **“generating a repair file that predicts said at least one of said fuses programmed for said repair”**. This phrase is not adequately defined.
39. Claim 18 states **“said first circuit is further configured to provide an elevation of said fuses at least one level of abstraction in said design”**. This phrase is not adequately defined.
40. Claim 19 states **“said first circuit is further configured to collect data relevant to said fuses that are grouped”**. This phrase is not adequately defined.

Claim Rejections - 35 USC § 112-Fourth Paragraph-dependent

41. The following is a quotation of the fourth paragraph of 35 U.S.C. 112: Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and

then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

42. Claim 3 (amended) states “method according to claim 14”. Note that claim 14 is not “previously set forth” relative to dependent claim 3. Thus, Claim 3 is rejected as an improper dependent claim. However, in the interests of “compact prosecution”, the Examiner will examine Claim 3 despite this technical problem.

Claim Rejections - 35 USC § 103

43. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
44. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
45. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable.
46. **Claim 1 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian.
47. Claim 1 (amended) is an independent claim with 3 limitations.
48. A-“**enumeration of a plurality of fuses**” is disclosed by Applicant's Admission at Specification Page 1 line 11 “Conventional methods exist to automate enumeration of all fuse locations on a die”. Note that *Constant v. Advanced Micro-Devices*, 848 F.2d 1560, 1570, 7 USPQ2d 1057, 1063 (Fed. Cir. 1988) states that Applicant's “own admission during prosecution...is binding upon him”.

49. **B-“compiling data for each one of said plurality of fuses, wherein said data comprises simulation path data”** is admitted by Applicant at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations...Conventional verilog simulation paths are derived by manual translation”.
50. Note that MPEP 2144.04(III) states “broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art.” Further, In re Venner, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states “it is well settled that it is not “invention” to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result.” Further, Constant v. Advanced Micro-Devices, 848 F.2d 1560, 1570, 7 USPQ2d 1057, 1063 (Fed. Cir. 1988) states that Applicant’s “own admission during prosecution...is binding upon him”.
51. Applicant’s Admissions apparently does not expressly disclose the remaining limitation.
52. **C-“simulating said design with at least one of said fuses programmed for said repair to verify said repair”** is disclosed by Kablanian at Column 2 lines 5-11, “External software is used to determine the optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip of selective removal through convention laser beam techniques to repair a defective memory cell”.
53. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5.
54. **Claim 2 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Tzori.
55. Claim 2 (amended) depends from Claim 1 (amended) with one additional limitation.
56. Applicant’s Admission does not appear to expressly disclose the additional limitation.
57. **“simulation path data comprises verilog simulation path data”** is disclosed by Tzori at Column 1 line 28 “Performing a Verilog simulation requires that a digital logic

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designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules”.

58. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Tzori to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype” according to Tzori Column 1 line 41.
59. **Claim 3 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.
60. Claim 3 (amended) depends from Claim 14 with one additional limitation.
61. Applicant’s Admission does not appear to expressly disclose the additional limitation.
62. **“said schematic path data comprises schematic paths, properties, hierarchy and a verilog path”** is disclosed by Tzori at Column 1 line 28 “Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules”.
63. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Tzori to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype” according to Tzori Column 1 line 41.
64. **Claim 4 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Sample.
65. Claim 4 (amended) depends from Claim 1 (amended) with one additional limitation.

66. Applicant's Admission does not appear to expressly disclose the additional limitation.
67. **"step (B) further comprises the sub-step of: generating a list of layout coordinates and schematic instance paths as part of said compiling"** is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE".
68. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Sample to modify Applicant's Admission. One of ordinary skill in the art would have been motivated to do this to "determine the optimal utilization" according to Kablanian at Column 2 line 5, and "the transistor list or layout specification is used to bum [sic] fuses" according to Sample at Column 1 line 46.
69. **Claim 5 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian.
70. Claim 5 (amended) depends from Claim 1 (amended) with one additional limitation.
71. **"generating a fuse report"** is disclosed by Applicant's Admission at Page 1 line 14 "Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time". Merriam-Webster's Collegiate Dictionary Tenth Edition defines "report" as "to give an account of : RELATE...to describe as being in a specified state". Thus, note that each "manual association" is a "fuse report" for a single fuse. Further, even if "report" were interpreted to require a report of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states "It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced".
72. **Claim 6 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian.
73. Claim 6 (amended) depends from Claim 5 (amended) with one additional limitation.
74. **"listing physical location of one or more devices in response to said fuse reports"** is disclosed by Applicant's Admission at Page 1 line 14 "Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time". Merriam-Webster's Collegiate Dictionary Tenth Edition defines "report" as

“to give an account of : RELATE...to describe as being in a specified state”. Thus, note that each “manually associate” constitutes a “fuse report” for a single fuse. Further, even if “report” were interpreted to require a report of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states “It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced”.

75. **Claim 7 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.
76. Claim 7 (amended) depends from Claim 1 (amended) with one new limitation.
77. **“generating a repair file that predicts said at least one of said fuses programmed for said repair”** is disclosed by Applicant’s Admission at Page 1 line 14 “Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time”. Merriam-Webster’s Collegiate Dictionary Tenth Edition defines “file” as “a collection of related data records”. Thus, note that each “manual association” is a “file” for a single fuse. Further, even if “file” were interpreted to require a file of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states “It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced”.
78. **Claim 8 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Higgins.
79. Claim 8 (amended) depends from Claim 7 (amended) with one additional limitation.
80. **“creating a repair program in response to said repair file”** is disclosed by Higgins Column 1 line 20 “Location information is then supplied to a controller for a laser repair device, which achieves a hardware fix.”
81. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Higgins to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal

utilization” according to Kablanian at Column 2 line 5, and because “repair procedures result in higher yields” according to Higgins Column 1 line 24.

82. **Claim 9 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Higgins.

83. Claim 9 (amended) depends from Claim 8 (amended) with one additional limitation.

84. **“verifying a function of said design in response to said repair program”** is disclosed by Tzori at Column 1 line 17 “Various different software and hardware systems exist for simulating and/or emulating”.

85. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Higgins to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “repair procedures result in higher yields” according to Higgins Column 1 line 24, and because “Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype” according to Tzori Column 1 line 41.

86. **Claim 10 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Higgins.

87. Claim 10 (amended) depends from Claim 8 (amended) with one additional limitation.

88. **“listing an output of said repair program as a list of coordinates for said at least one of said fuses programmed for said repair in terms of a plurality of logical addresses”** is disclosed by Applicant’s Admission at Page 1 line 14 “Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time”.

89. **Claim 11 (amended) is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Higgins and Official Notice.

90. Claim 11 (amended) depends from Claim 10 (amended) with one new limitation.

91. **“storing said coordinates in a memory”** is disclosed by is disclosed by Official Notice that it is well known in the art to store coordinates in memory for future use or to create a permanent record.

92. Applicant is entitled to traverse the official notice according to MPEP § 2144.03.

However, MPEP § 2144.03 further states “See also *In re Boon*, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice).” Specifically, *In re Boon*, 169 USPQ 231, 234 states “as we held in *Ahlert*, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or repute of the reference cited in support of the assertion. **We did not mean to imply by this statement that a bald challenge, with nothing more, would be all that was needed**”. Further note that 37 CFR § 1.671(c)(3) states “Judicial notice means official notice”. Thus, a traversal by the Applicant that is merely “a bald challenge, with nothing more” will be given very little weight.

93. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Higgins and Official Notice to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “repair procedures result in higher yields” according to Higgins Column 1 line 24, and to store coordinates in memory for future use or to create a permanent record according to Official Notice.

94. **Claim 12 (amended) is rejected** under 35 U.S.C. 103(a).

95. Claim 12 (amended) is an independent “apparatus” claim with the same limitations as Claim 1, and thus is rejected for the same reasons.

96. **Claim 13 (amended) is rejected** under 35 U.S.C. 103(a).

97. Claim 13 (amended) is an “apparatus” claim with “means for” language and with the same limitations as Claim 1, and thus is rejected for the same reasons.

98. **Claim 14 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.

99. Claim 14 depends from Claim 1, with one additional limitation.

100. **“said data further comprises schematic path data”** is disclosed by Applicant’s Admission at Specification Page 1 line 16, “The conventional methods to manually

associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.”

101. **Claim 15 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.
102. Claim 15 depends from Claim 1, with one additional limitation.
103. **“said data further comprises physical layout data”** is disclosed by Applicant’s Admission at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.”
104. **Claim 16 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.
105. Claim 16 depends from Claim 1, with one additional limitation.
106. **“mapping a plurality of co-ordinates of said fuses to a plurality of verilog statements”** is disclosed by Applicant’s Admission at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.”
107. **Claim 17 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Tzori.
108. Claim 17 depends from Claim 1, with one additional limitation.
109. **“checking said repair file and said repair program for an error”** is disclosed by is disclosed by Tzori at Column 1 line 17 “Various different software and hardware systems exist for simulating and/or emulating”.
110. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Tzori to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “Since in

almost all instances IC manufacturers simulate their designs before fabricating even a prototype” according to Tzori Column 1 line 41.

111. **Claim 18 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.
112. Claim 18 depends from Claim 12, with one additional limitation.
113. **“said first circuit is further configured to provide an elevation of said fuses at least one level of abstraction in said design”** is admitted by Applicant at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations...Conventional verilog simulation paths are derived by manual translation”.
114. **Claim 19 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.
115. Claim 19 depends from Claim 12, with one additional limitation.
116. **“said first circuit is further configured to collect data relevant to said fuses that are grouped”** is admitted by Applicant at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations...Conventional verilog simulation paths are derived by manual translation”.
117. **Claim 20 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Official Notice.
118. Claim 20 depends from Claim 12, with one additional limitation.
119. **“said second circuit is further configured to write a report file”** is disclosed by is disclosed by Applicant’s Admission at Page 1 line 14 “Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time”. Merriam-Webster’s Collegiate Dictionary Tenth Edition defines “report” as “to give an account of : RELATE...to describe as being in a specified state”. Thus, note that each “manually associate” constitutes a “fuse report” for a single fuse. Further, even if “report” were interpreted to require a report of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states “It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced”.

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120. Additionally, writing files is disclosed by Official Notice that it is well known in the art to write files for future use or to create a permanent record.

121. Applicant is entitled to traverse the official notice according to MPEP § 2144.03. However, MPEP § 2144.03 further states “See also *In re Boon*, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice).” Specifically, *In re Boon*, 169 USPQ 231, 234 states “as we held in *Ahlert*, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or repute of the reference cited in support of the assertion. **We did not mean to imply by this statement that a bald challenge, with nothing more, would be all that was needed**”. Further note that 37 CFR § 1.671(c)(3) states “Judicial notice means official notice”. Thus, a traversal by the Applicant that is merely “a bald challenge, with nothing more” will be given very little weight.

122. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Official Notice to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and to write files for future use or to create a permanent record according to Official Notice.

Response to Substantial Amendments-FINAL OFFICE ACTION

123. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

124. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

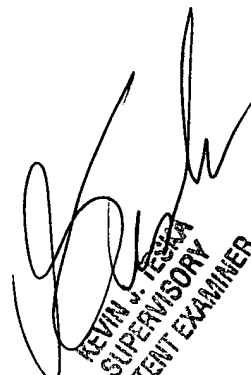
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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

125. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM.
126. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:
127. (703) 746-7238 --- for communications after a Final Rejection has been made;
128. (703) 746-7239 --- for other official communications; and
129. (703) 746-7240 --- for non-official or draft communications.
130. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *


KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER